SolidRun

SR-uSOM-MX6 Application Note

Connecting Parallel Camera

Document rev 1.0

Documentation Revision History

Date	Owner	Changes	Notes
23-April-2014	Rabeeh Khoury	Initial	Initial release

Introduction

The SolidRun SR-uSOM-MX6 is a high performance micro system on module that is based on the highly integrated Freescale i.MX6 family of products.

This application note provides information on signal mux and pinout to be used when integrating SR-uSOM-MX6 with a parallel camera sensor.

Please refer to the SR-uSOM-MX6 Reference Manual for detailed hardware integration manual.

It is highly recommended to refer to the Freescale io-mux utility and Freescale i.MX6 reference manual for more details.

The design of the SR-uSOM-MX6 incorporates 3 board to board headers that expose to a carrier board most of the functions of the different flavors of the Freescale i.MX6 family of SoC.

Besides the dedicated MIPI CSI-2 serial interface, there is an option to connect a camera with parallel interface. Internally in the i.MX6 device it connects to the –

1. **IPU1 CSI1** when using the solo or dual lite versions of the devices.
2. **IPU2 CSI1** when using the dual or quad versions of the devices.

In the pinout table below, when referring to the IPUx_CSI1_DATA00, it should be referred as IPU1_CSI1_DATA00 on the solo or dual lite versions, and as IPU2_CSI1_DATA00 on the dual or quad versions.

Pinout Description

The pinout that is exposed on the SR-uSOM-MX6 board to board headers are as follows –

Signal Name	Board To Board Header Name	Pin Number	Orcad Port Signal Name	i.MX6 Ball Number
IPUx_CSI1_DATA00	Main	66	DISP1_DATA00	M21
IPUx_CSI1_DATA01	Main	60	DISP1_DATA01	L24
IPUx_CSI1_DATA02	Main	56	DISP1_DATA02	L25
IPUx_CSI1_DATA03	Main	54	DISP1_DATA03	K25
IPUx_CSI1_DATA04	Main	64	DISP1_DATA04	L23
IPUx_CSI1_DATA05	Main	62	DISP1_DATA05	L22
IPUx_CSI1_DATA06	Main	58	DISP1_DATA06	K24
IPUx_CSI1_DATA07	Third	70	DISP1_DATA07	L21
IPUx_CSI1_DATA08	Third	55	DISP1_DATA08	J25
IPUx_CSI1_DATA09	Third	60	DISP1_DATA09	L20
IPUx_CSI1_DATA10	Third	57	DISP1_DATA10	K23
IPUx_CSI1_DATA11	Third	68	DISP1_DATA11	K21
IPUx_CSI1_DATA12	Third	59	DISP1_DATA12	G24
IPUx_CSI1_DATA13	Third	64	DISP1_DATA13	J22
IPUx_CSI1_DATA14	Third	63	DISP1_DATA14	G25
IPUx_CSI1_DATA15	Third	62	DISP1_DATA15	H22
IPUx_CSI1_DATA16	Third	66	DISP1_DATA16	H23
IPUx_CSI1_DATA17	Third	69	DISP1_DATA17	F24
IPUx_CSI1_DATA18	Third	56	DISP1_DATA18	J21
IPUx_CSI1_DATA19	Third	67	DISP1_DATA19	F25
IPUx_CSI1_DATA_EN	Third	43	DI1_PIN15	M22
IPUx_CSI1_HSYNC	Third	41	DI1_PIN02	M20
IPUx_CSI1_PIXCLK	Third	54	DI1_DISP_CLK	H25
IPUx_CSI1_VSYNC	Third	51	DI1_PIN03	M24