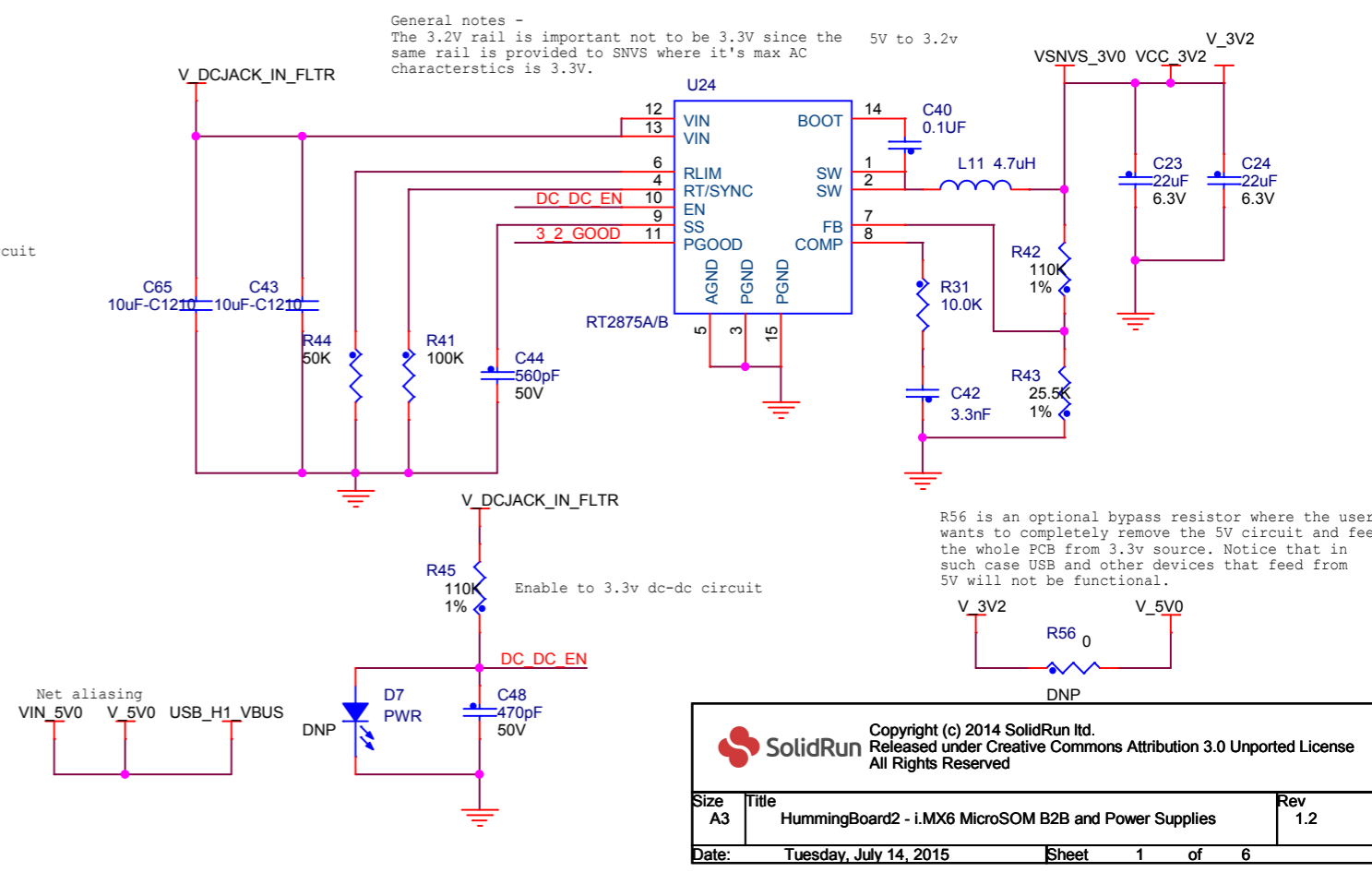
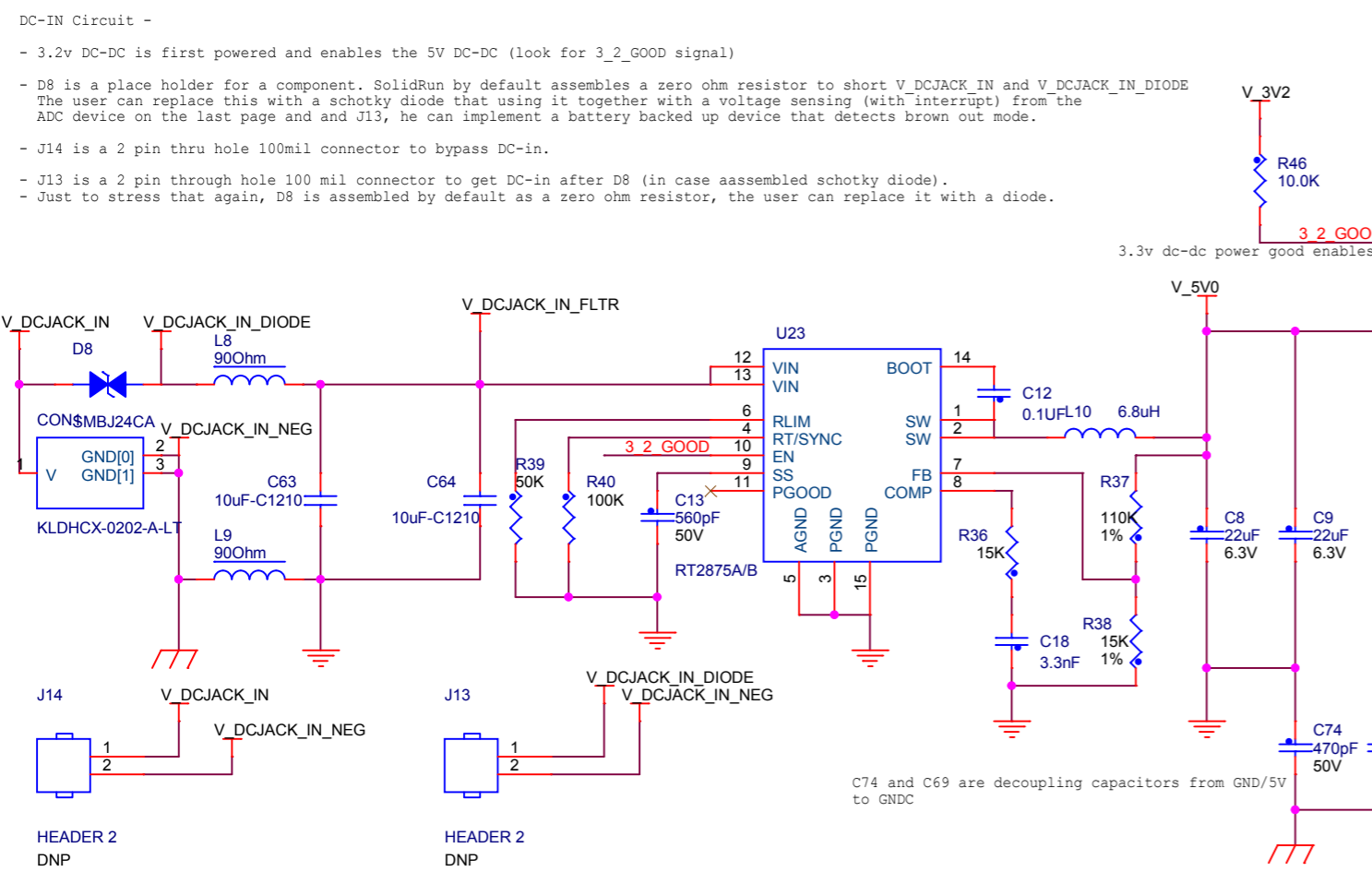
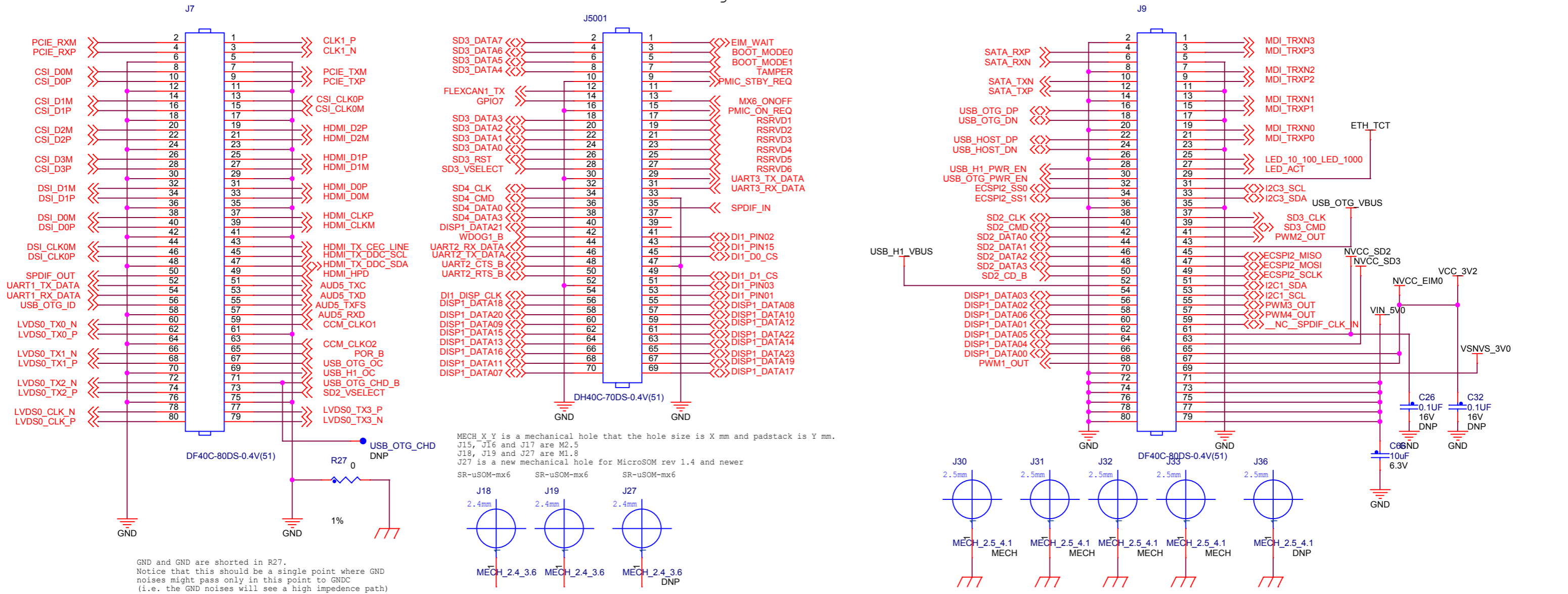
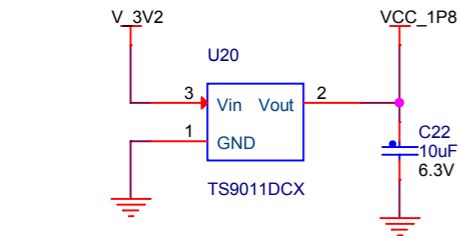


HummingBoard 2 Schematics rev 1.2

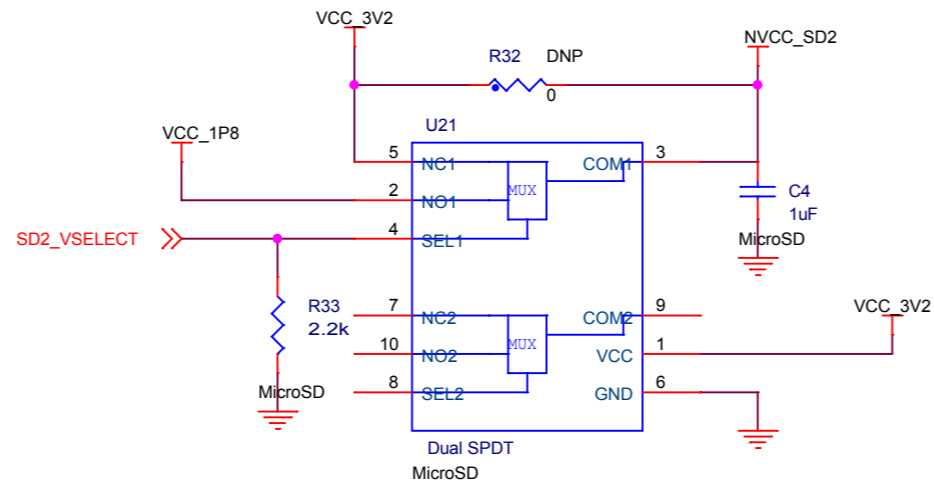


Analog audio and micro SD 1.8v interface support LDO

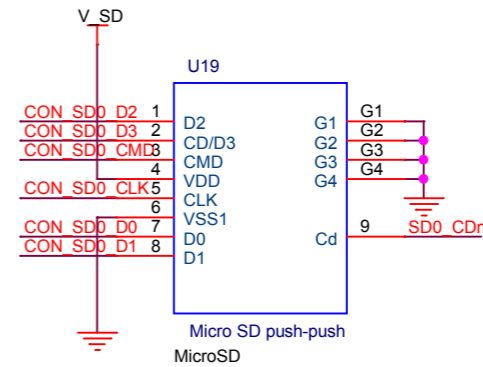


LDO input capacitor is shared with USB hub filter

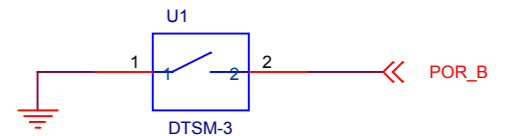
micro SD 3.2v/1.8v interface voltage switcher circuitry



micro SD interface

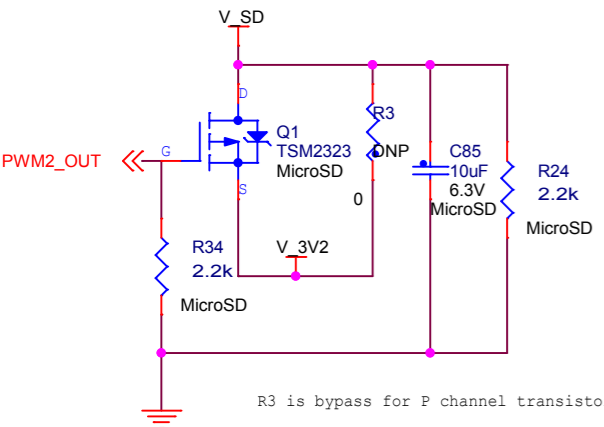


RESET button



micro SD power on/off

Some micro SD cards don't report UHS-1 support after warmboot. This power cycle circuitry is intended to power cycle those kind of micro SD cards so that they would report UHS-1 support.

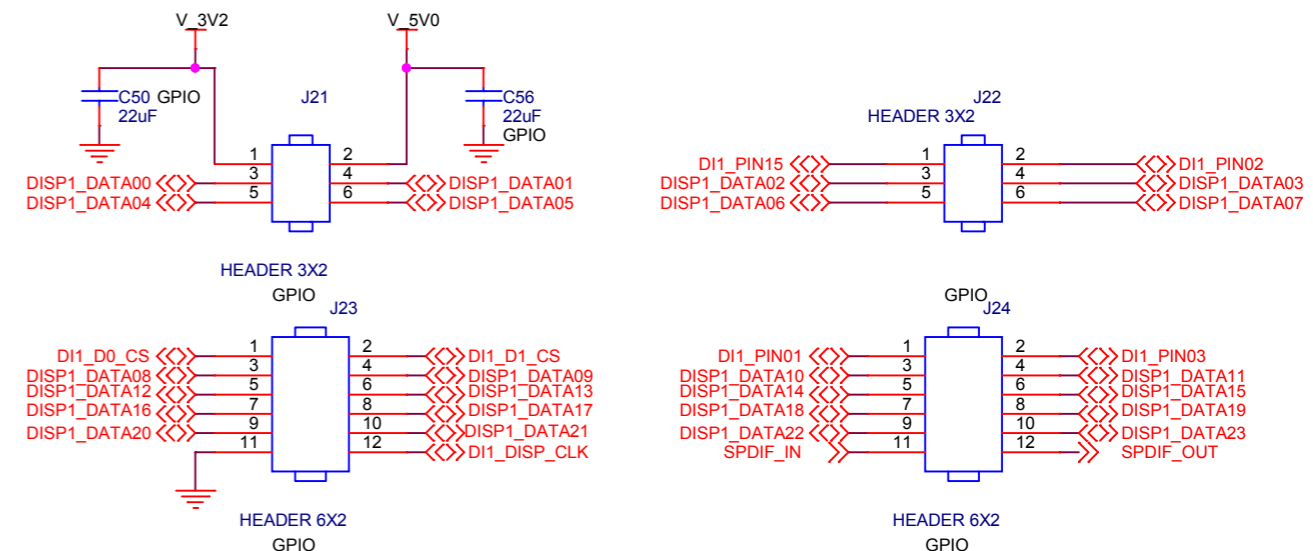


R3 is bypass for P channel transistor

36 pin GPIO header notes -

- The header mainly exposes the parallel port display out / camera in header (can be muxed to other functions) with other signals that can be used as SPDIF in/out
- The pins also decides the boot device. So notice not to randomly pull up/down those pins without referring to the i.MX6 reference manual documentation.
- Those pins can be pulled up/down freely in case the i.MX6 device fuses are blown in a manner to indicate to the processor to boot from it's internal fuse settings. In such a case the user can pull up/down any of those pins freely.
- By default the Linux kernel device tree sets those pins as GPIOs.
- Notice how the pins order on the header, DISP1_DATA0, DATA1 ... DATA23

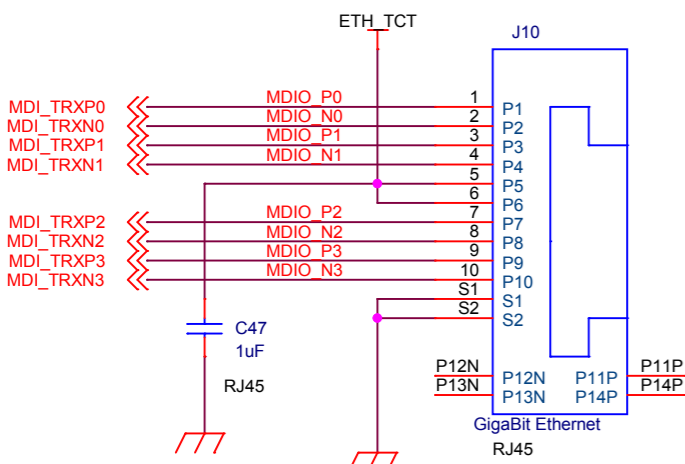
36 pin header implemented using 4 headers



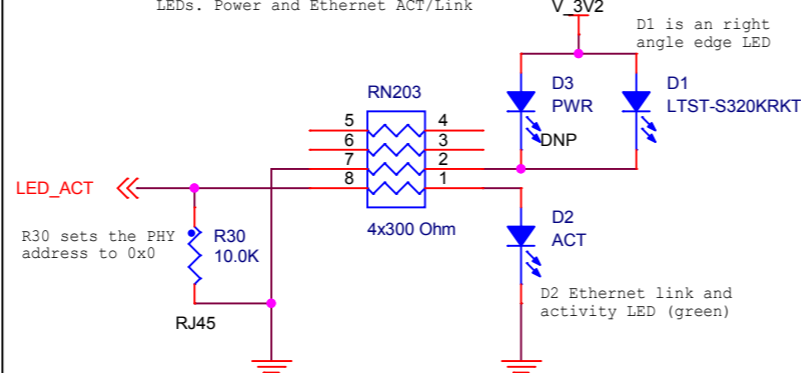
Test points (refer to the layout about their places)

- WD0G1_B >> T1 DNP
- GPIO7 >> T2 DNP
- EIM_WAIT <<> T3 DNP
- MX6_ONOFF >> T5 DNP
- PMIC_ON_REQ <<> T6 DNP
- PMIC_STBY_REQ <<> T7 DNP
- TAMPER >> T8 DNP
- USB_OTG_ID >> T9 DNP

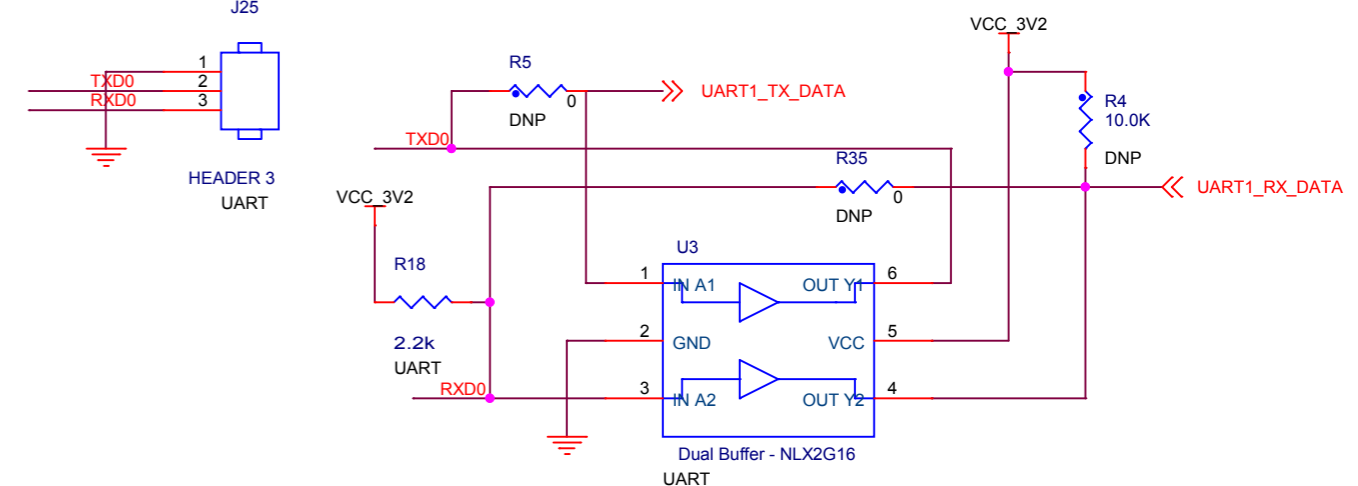
RJ45 Connector

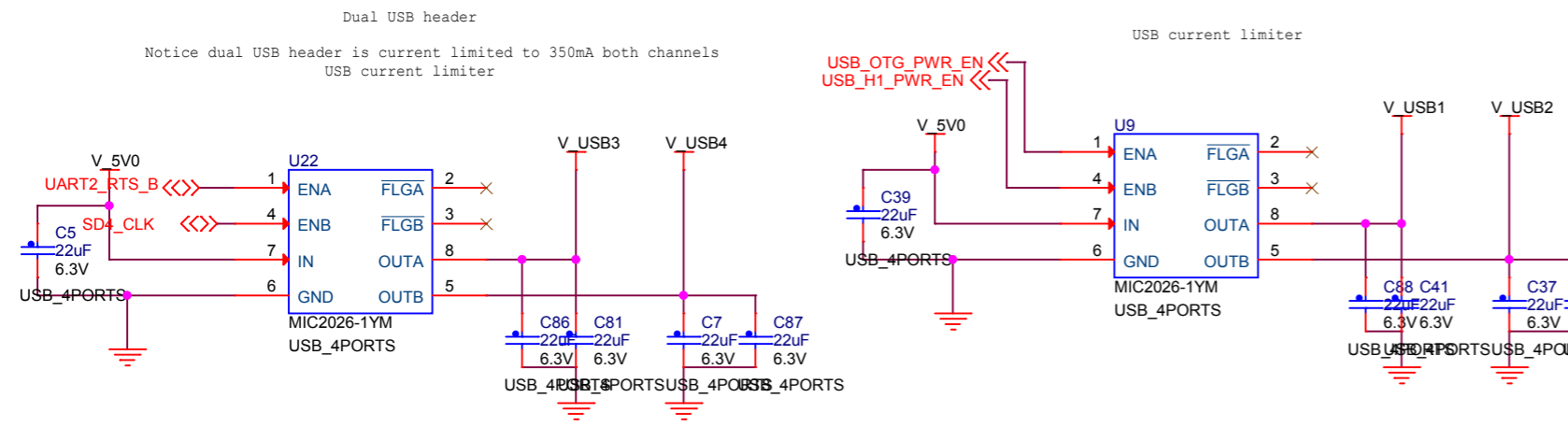


LEDs. Power and Ethernet ACT/Link



Buffered UART header (main debug console)



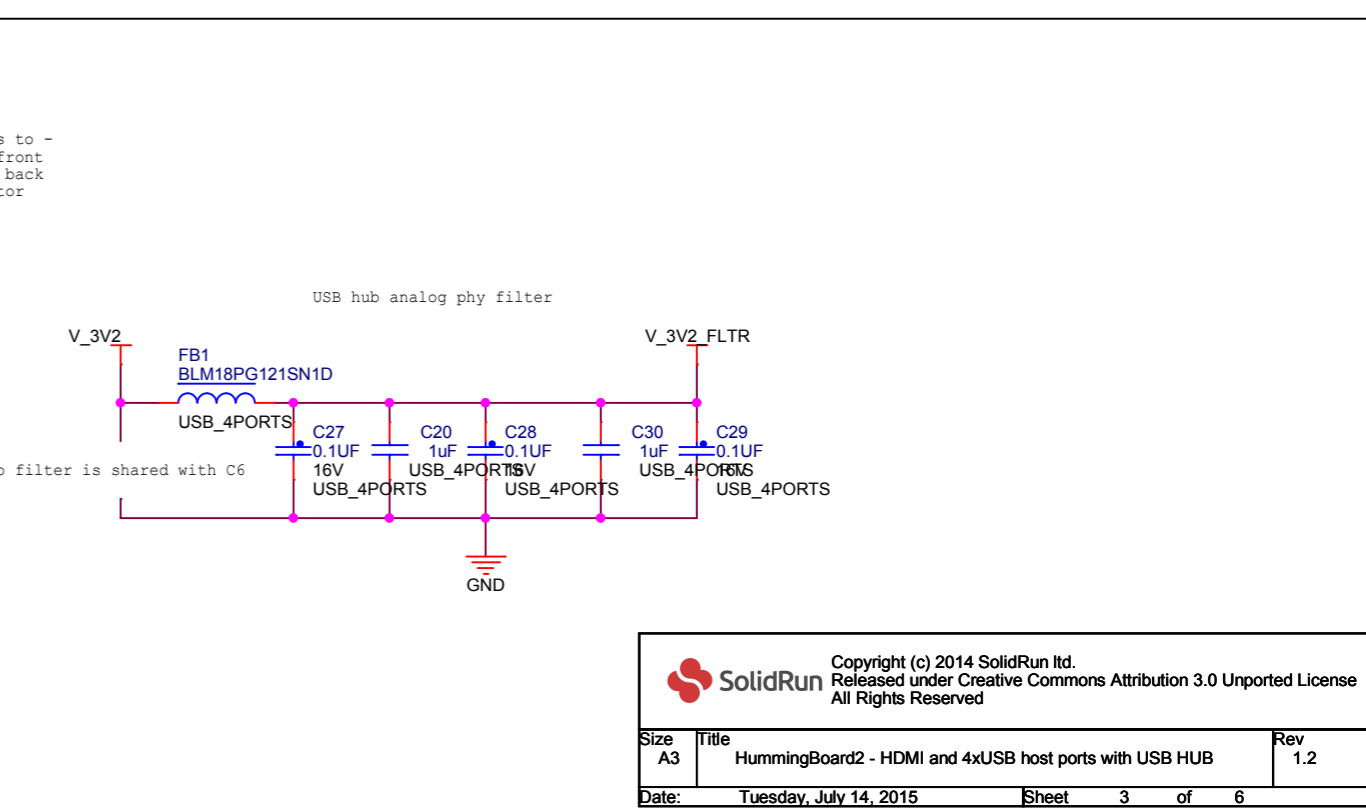
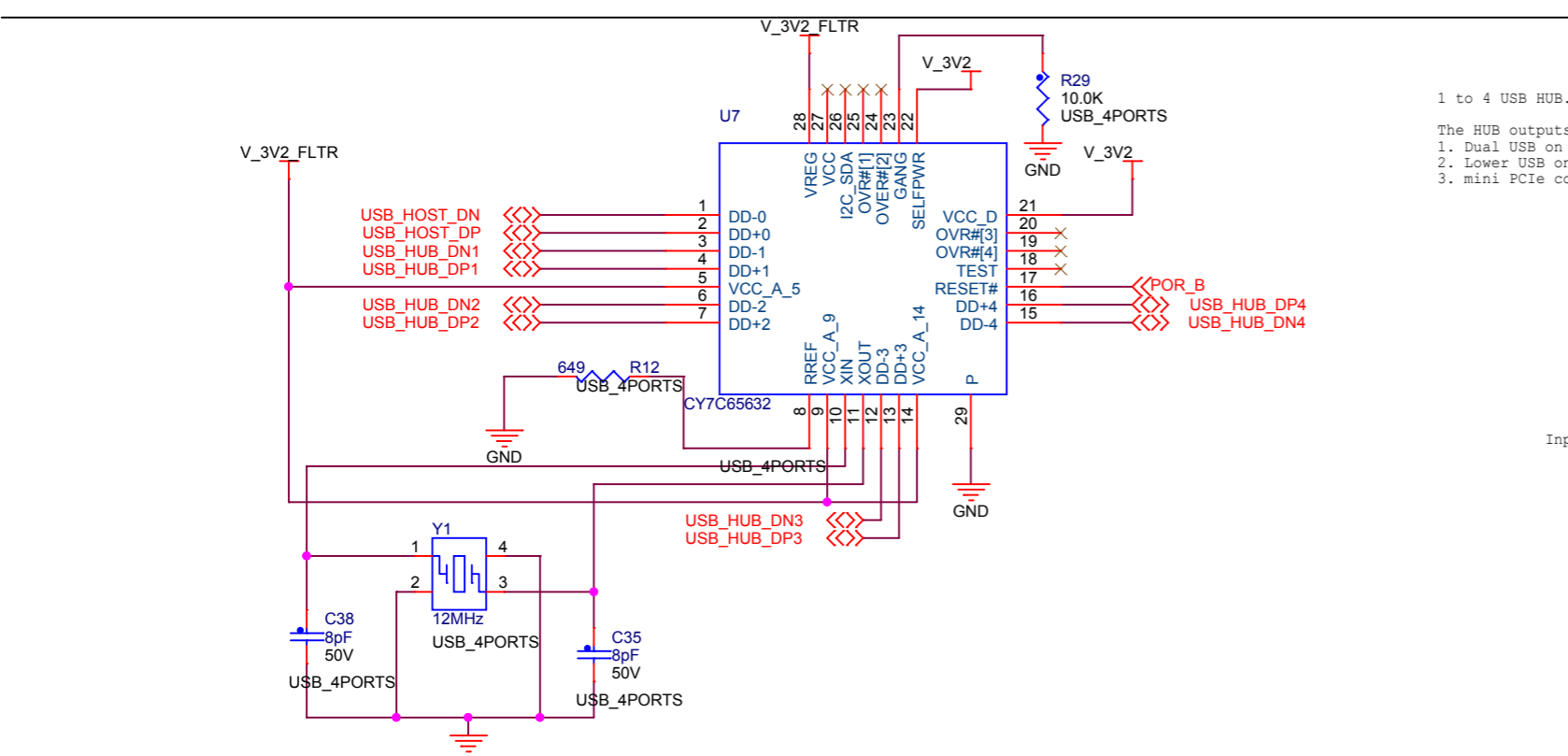
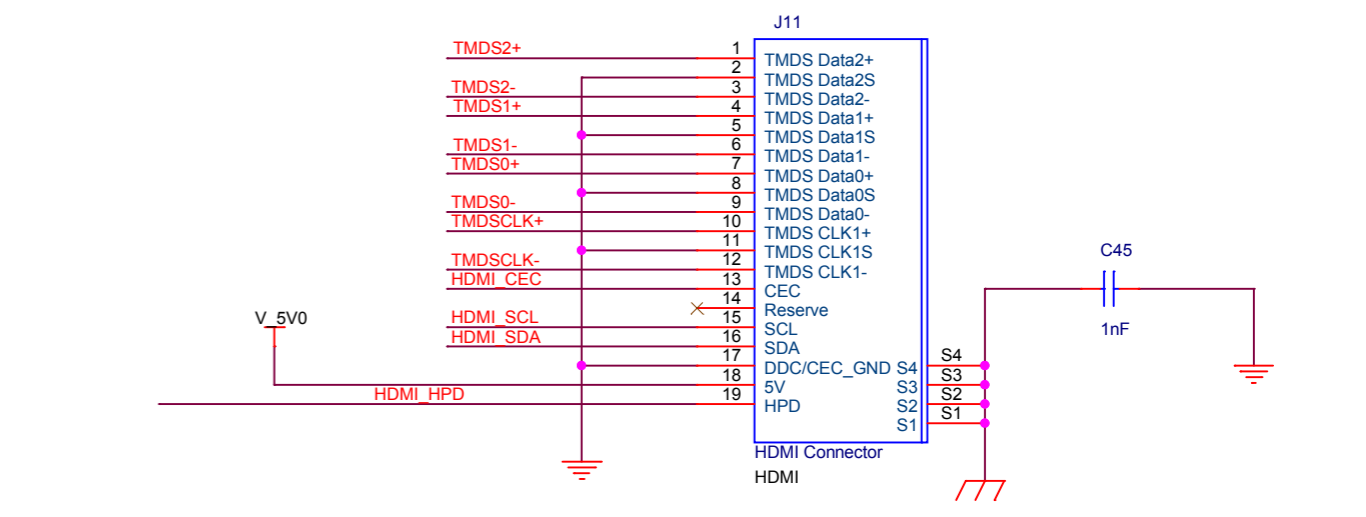
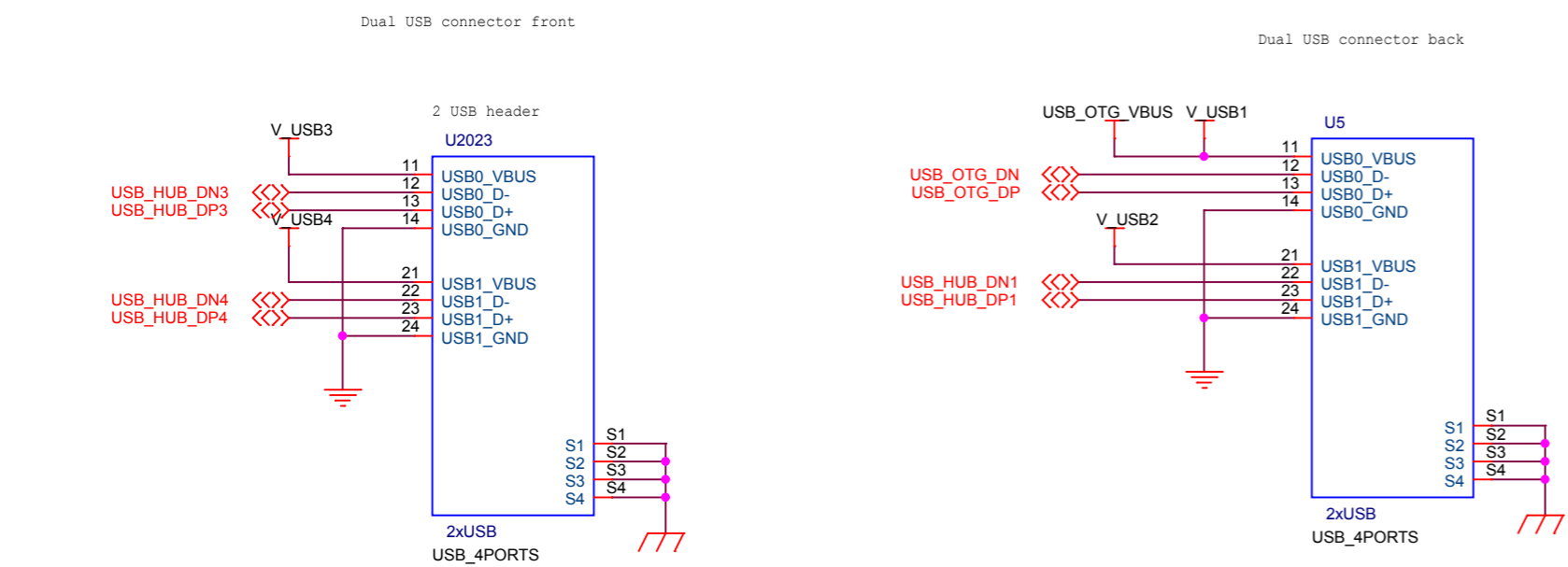
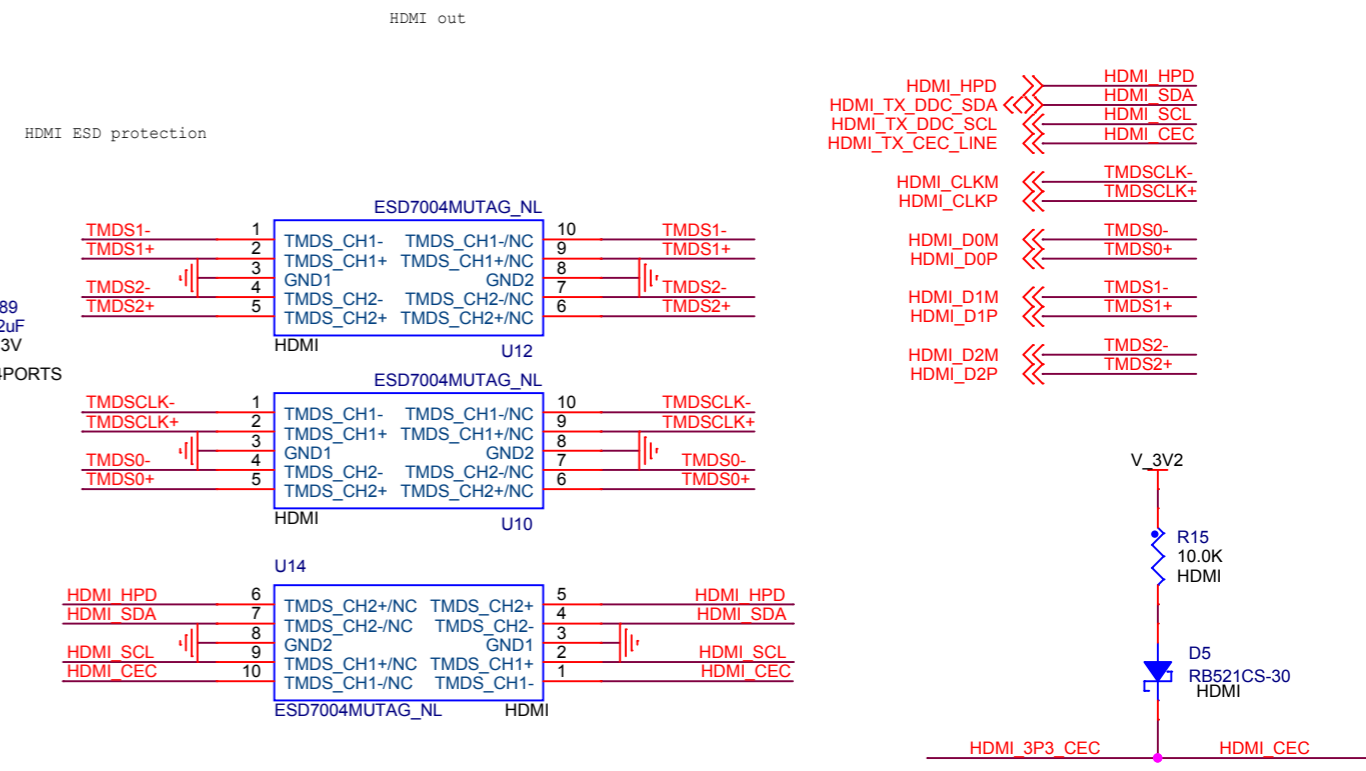


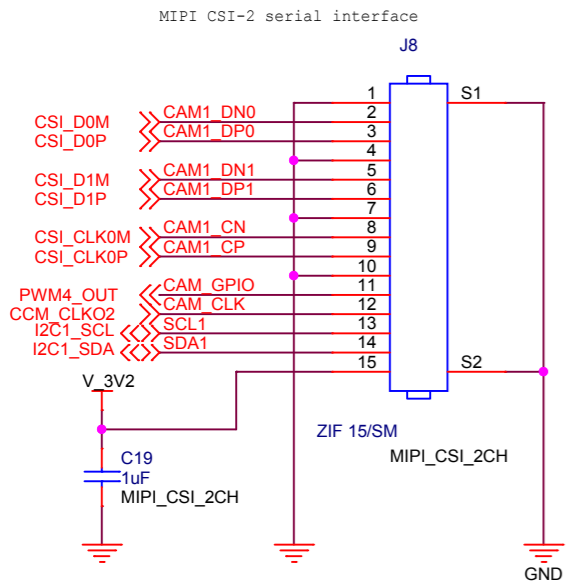
GPIO pin mapping -

Pin	GPIO
OTG (ENA)	(3, 22)
H1 (ENB)	(1, 0)

GPIO pin mapping -

Pin	GPIO
OTG (ENA)	(3, 22)
H1 (ENB)	(1, 0)

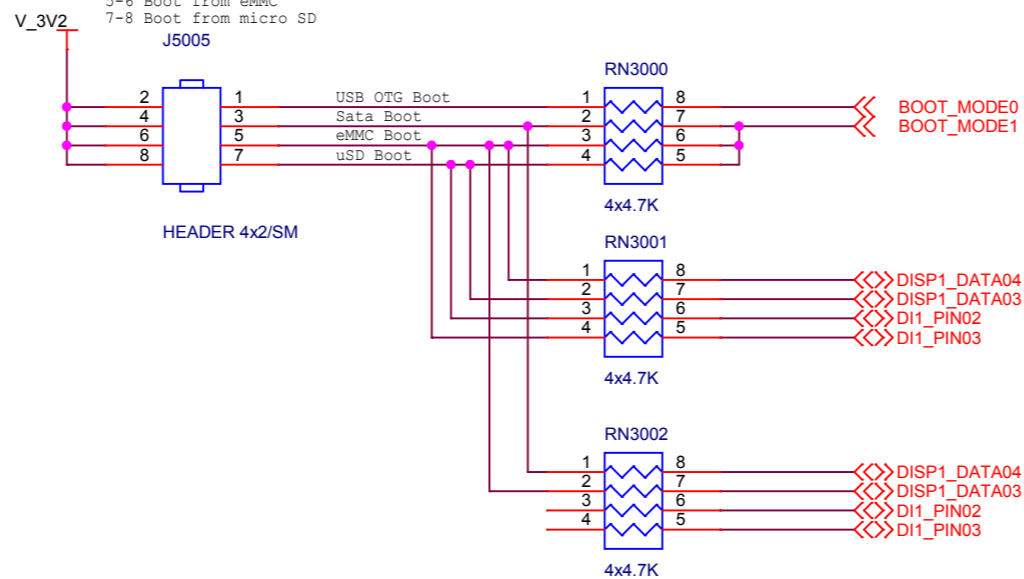




Boot select uses 3rd header pinout to select boot device.
 Notice that i.MX6 without boot from fuse must be used;
 otherwise the boot device is chosen with whatever
 the i.MX6 fuses selects

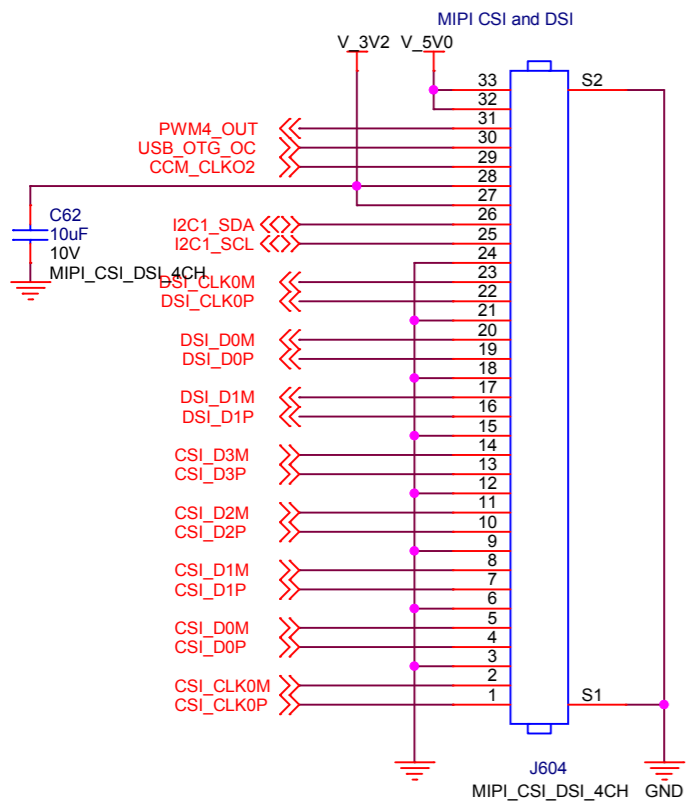
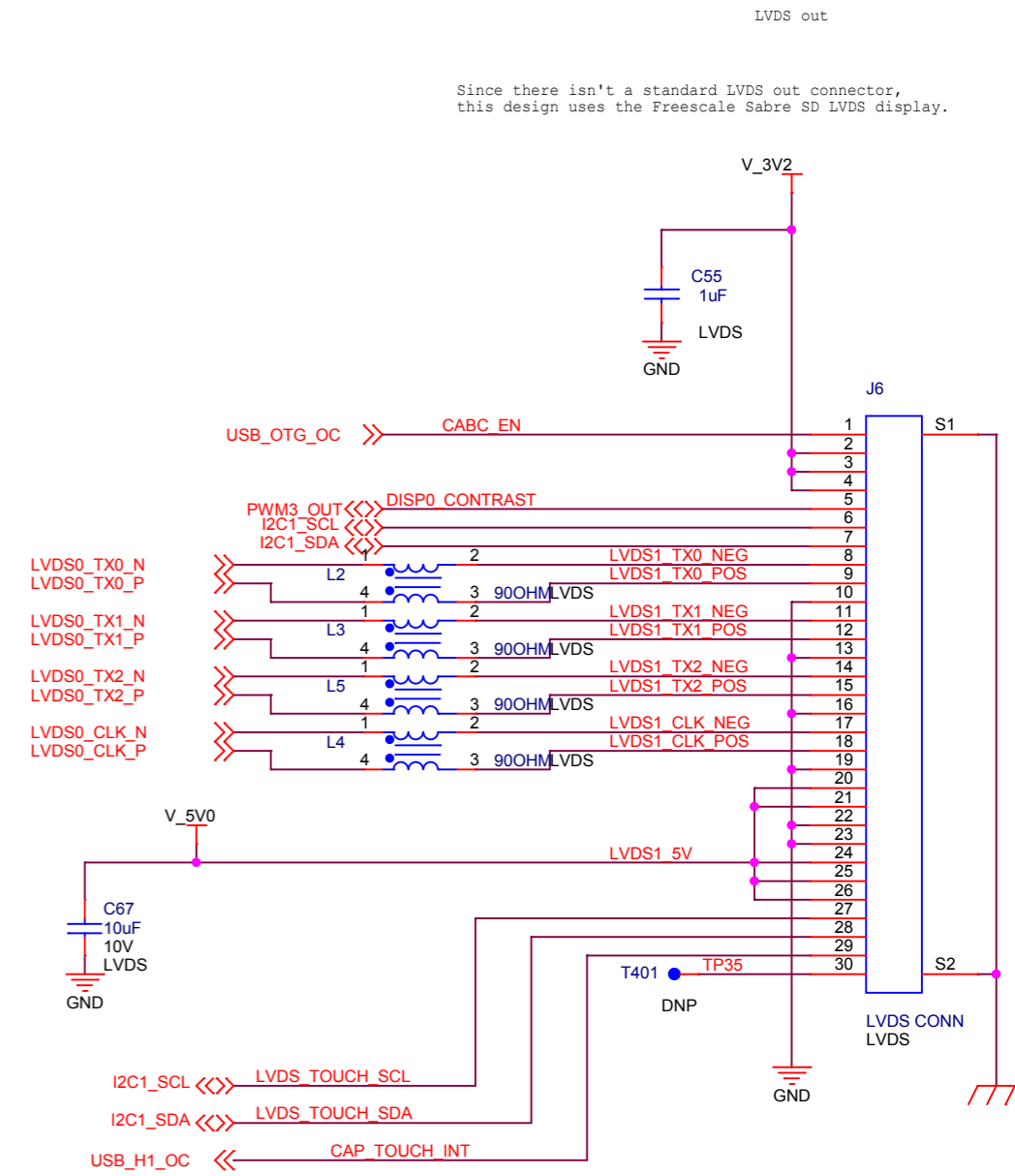
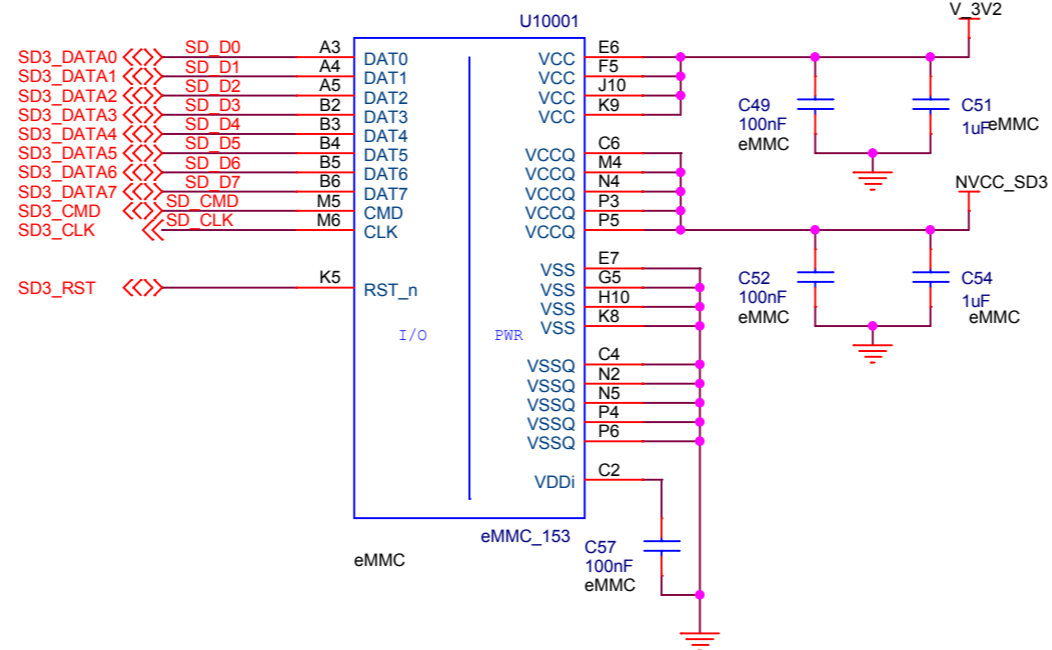
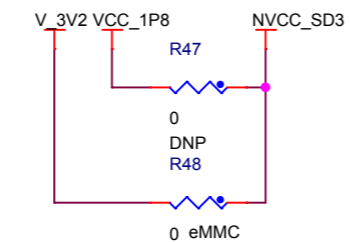
From usage point of view, the user can use a jumper to
 bridge only a single configuration from the 2x4 J5005 header -

1-2 USB OTG boot (you need an external PC to boot)
 3-4 Boot from SATA
 5-6 Boot from eMMC
 7-8 Boot from micro SD

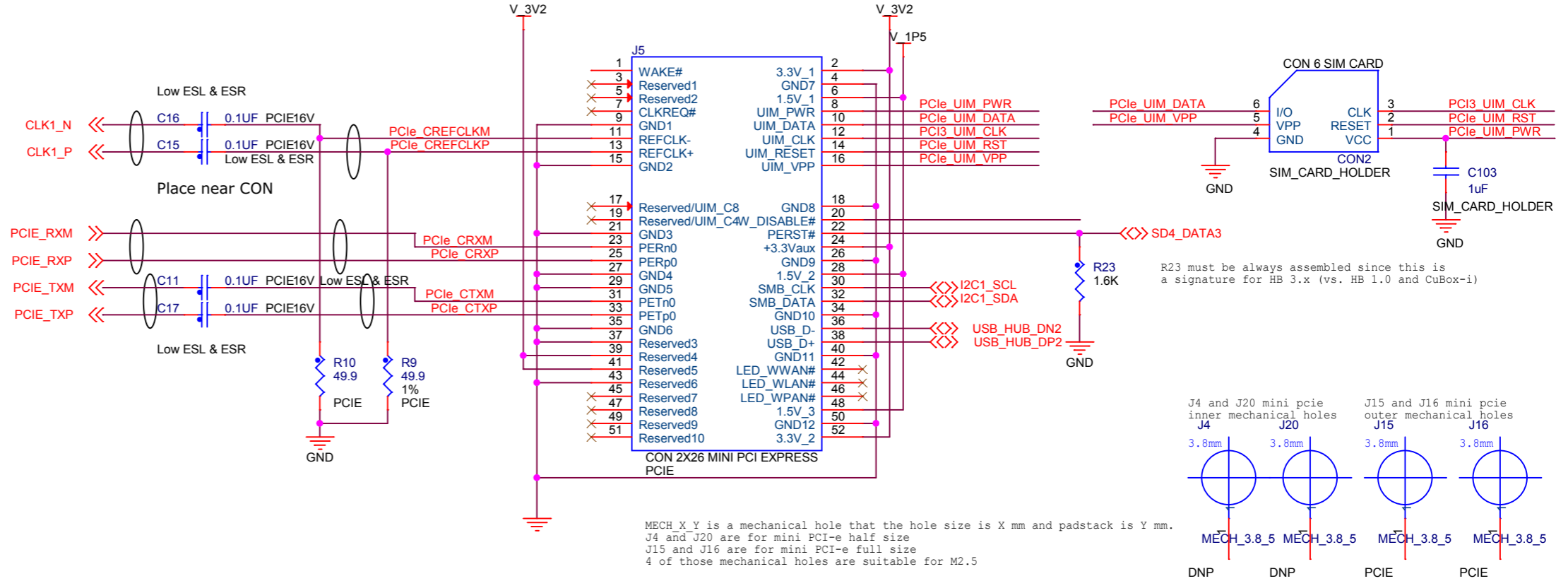
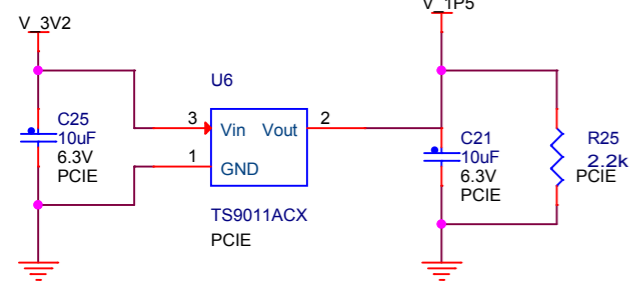


eMMC

eMMC VCCQ is 3.2v



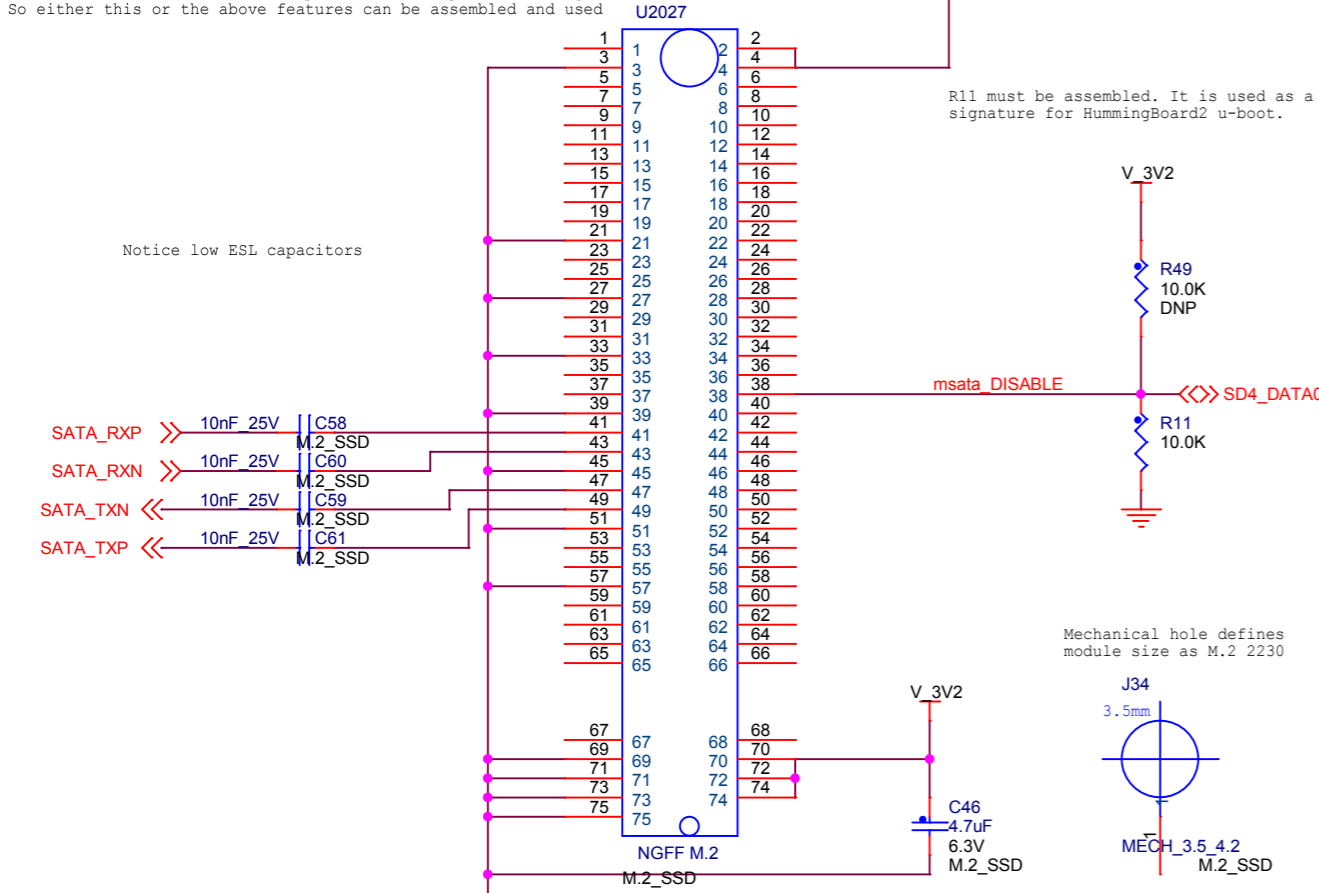
3.3v to 1.5v LDO (for mini pci express)



R23 must be always assembled since this is a signature for HB 3.x (vs. HB 1.0 and CuBox-i)

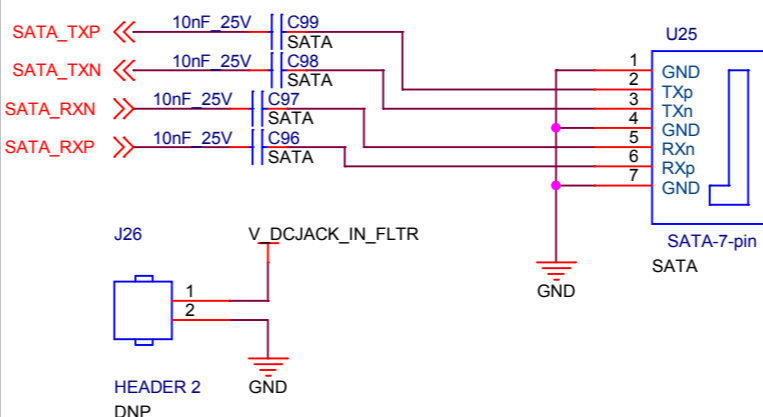
M.2 SSD connector

The mechanical hole defines it as M.2 2230 form factor wise. it can be used with i.MX6 dual / quad SoCs since only both those have SATA function. Notice that this M.2 SSD overlaps with SATA 7 pin to the right.



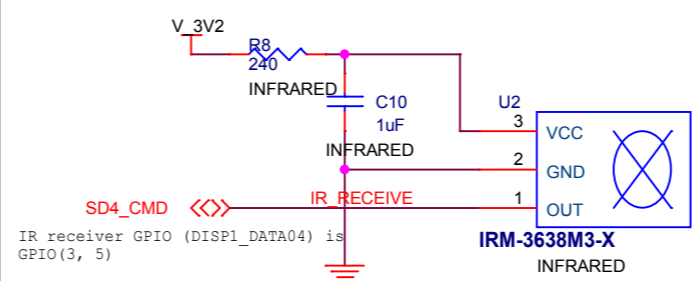
SATA connector with power

Notes -
 1. This feature overlaps with M.2 SSD on the left. So either this or M.2 can be assembled and used.
 2. Notice J26 is adjacent to U10002 pins 15 and 16. U10002 pins 15,16 and J26 can assemble together a 100 mil SATA HDD 12v and 5v power cable connector when V_DCJACK_IN_FLTR is set as 12V, i.e. the user uses a 12V power supply.



Infra red receiver

240 ohm resistor required to minimize noises on DC in



R28 and C80 RC circuit here is required to avoid sudden drop of V_3V2 on PCF8523 (inserting and removing cards). Since PCF8523 samples the voltage every 1ms, such a drop might not be detected in time causing lost of date/time track (i.e. no switchover to battery)

